Order this document
by MC68HC11ED0TS/D

MC68HC11ED0

Technical Summary
8-Bit Microcontroller

1 Introduction

The MC68HC11ED0 is a low cost member of the M68HC11 family of microcontrollers. This MCU has a multiplexed address/data bus and is characterized by high speed and low power consumption. The fully static design allows operation at frequencies from 3 MHz to dc.

Pin count is minimized for cost-sensitive applications. Because there is no on-chip ROM, this device is optimized for expanded-bus systems. On-chip serial peripheral interface (SPI) and serial communications interface (SCI) provide a convenient means for transferring data to and from internal RAM. Refer to the block diagram.

1.1 Features

- M68HC11 CPU
- Power Saving STOP and WAIT Modes
- 512 Bytes RAM
- Multiplexed Address and Data Buses
- Enhanced 16-Bit Timer with Four-Stage Programmable Prescaler
  - Three Input Capture (IC) Channels
  - Four Output Compare (OC) Channels
  - One Additional Channel, Selectable as Fourth IC or Fifth OC
- 8-Bit Pulse Accumulator
- Real-Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog
- Clock Monitor
- Enhanced Asynchronous Nonreturn to Zero (NRZ) Serial Communications
- Enhanced Synchronous Serial Peripheral Interface (SPI)
- Eight Bidirectional Input/Output (I/O) Lines
- Three Input-Only Lines
- Three Output-Only Lines (One Output-Only Line in 40-Pin
- Available in 44-Pin Plastic Leaded Chip Carrier (PLCC), Dual In-Line Package (DIP) (All Packages are Plastic)

Table 1 Device Ordering Information

Package	Temperature	Description	Frequency	MC Order Number
44-Pin PLCC	– 40° to + 85° C	No ROM/EPROM, No EEPROM, 512 Bytes RAM	2 MHz	MC68HC11ED0CFN2
			3 MHz	MC68HC11ED0CFN3
	– 40° to + 105° C		2 MHz	MC68HC11ED0VFN2
			3 MHz	MC68HC11ED0VFN3
	– 40° to + 125° C		2 MHz	MC68HC11ED0MFN2
			3 MHz	MC68HC11ED0MFN3
44-Pin QFP	– 40° to + 85° C		2 MHz	MC68HC11ED0CFU2
			3 MHz	MC68HC11ED0CFU3
	– 40° to + 105° C		2 MHz	MC68HC11ED0VFU2
			3 MHz	MC68HC11ED0VFU3
	– 40° to + 125° C		2 MHz	MC68HC11ED0MFU2
			3 MHz	MC68HC11ED0MFU3
40-Pin DIP	– 40° to + 85° C		2 MHz	MC68HC11ED0CP2
			3 MHz	MC68HC11ED0CP3
	– 40° to + 105° C		2 MHz	MC68HC11ED0VP2
			3 MHz	MC68HC11ED0VP3
	– 40° to + 125° C		2 MHz	MC68HC11ED0MP2
			3 MHz	MC68HC11ED0MP3

Figure 1 Pin Assignments for 44-Pin PLCC

Figure 2 Pin Assignments for 44-Pin QFP

Figure 3 Pin Assignments for 40-Pin DIP

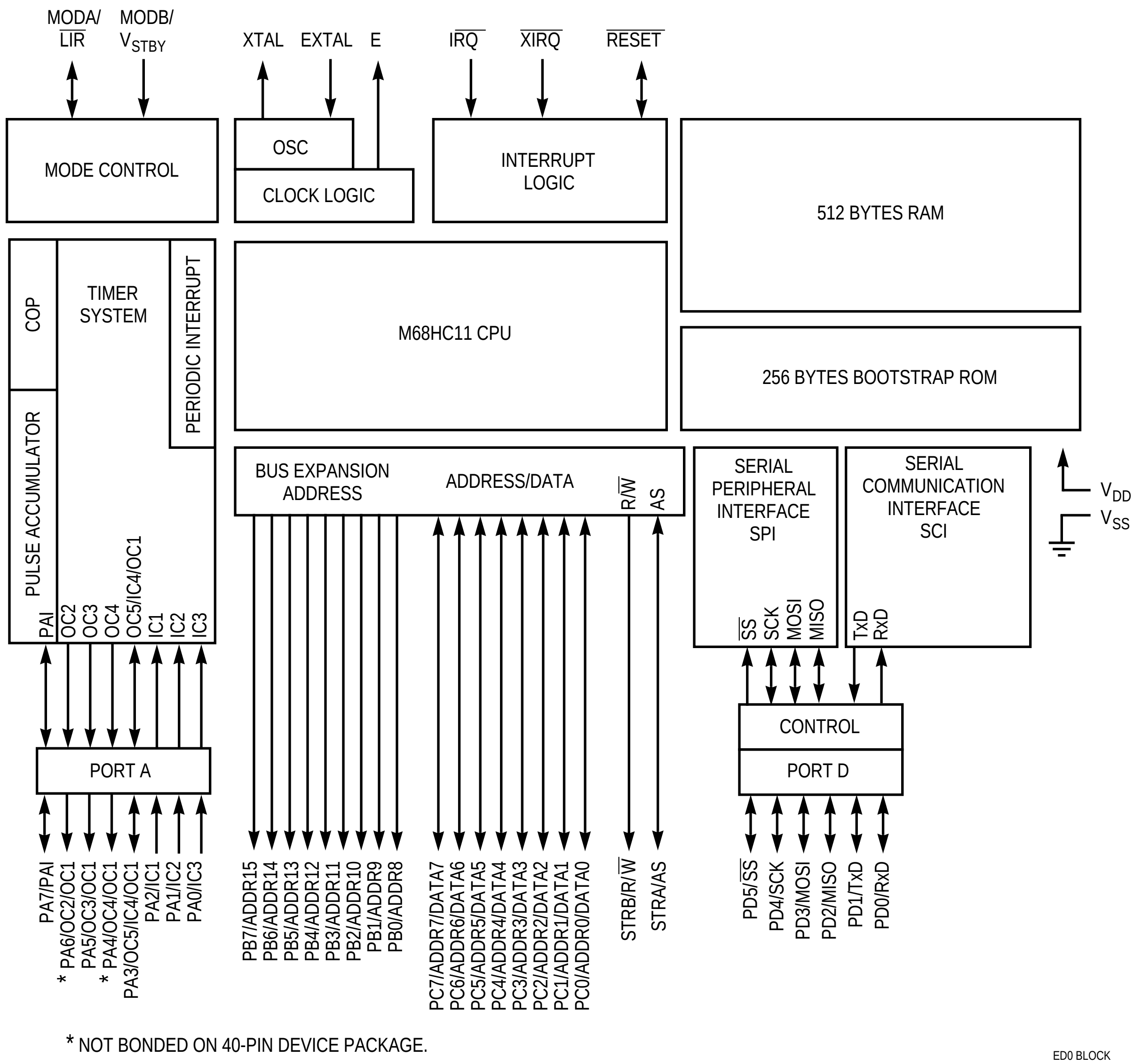

Figure 4 MC68HC11ED0 Block Diagram

TABLE OF CONTENTS (Continued)

Section **Page**

Register Index

2 Operating Modes

The MC68HC11ED0 MCU has three modes of operation. For expanded and special test modes, there are no reset or interrupt vectors contained in on-chip resources. An external memory must be used to provide vectors at locations $FFC0–$FFFF. In bootstrap mode a small on-chip ROM becomes present in the memory map and provides the vectors for this mode. Refer to the memory map diagram. The modes are described as follows.

2.1 Bootstrap Mode

Bootstrap mode allows special-purpose programs to be entered into internal RAM. The MCU contains 256 bytes of bootstrap ROM which is enabled and present in the memory map only when the device is in bootstrap mode. The bootstrap ROM contains a small program which initializes the SCI and allows the user to download exactly 256 bytes of code into on-chip RAM. After receiving the character for address $01FF, control passes to the loaded program at $0100. Vectors are present on-chip and located at $BFC0–$BFFF. Refer to the memory map diagram.

2.2 Special Test Mode

Special test mode is used primarily for factory testing. In this operating mode, vectors must be provided externally at $BFC0–$BFFF.

2.3 Expanded Operating Mode

In expanded operating mode, the MCU has a 64-Kbyte address range and, using the expansion bus, can access external resources within the 64-Kbyte space. This space includes on-chip memory addresses in addition to addressing capabilities for external peripheral and memory devices. Refer to the memory map diagram. In expanded operating mode, high order address bits are output on ADDR[15:8] pins, low order address bits and the data bus are multiplexed on ADDR/DATA[7:0]. Refer to the block diagram. The read/write ($R/\overline{W}$) and address strobe (AS) signals allow the low-order address and the eight-bit data bus to be time-multiplexed on the same pins. During the first half of each bus cycle address information is present. During the second half of each bus cycle the pins become the bidirectional data bus. AS is an active-high latch enable signal for an external address latch. Address information is allowed through the transparent latch while AS is high and is latched when AS drives low. The address, $R/\overline{W}$, and AS signals are active and valid for all bus cycles, including accesses to internal memory locations. The E-clock is used to enable external devices to drive data onto the internal data bus during the second half of a read bus cycle (E clock high). $R/\overline{W}$ controls the direction of data transfers. $R/\overline{W}$ drives low when data is being written to the external data bus. $R/\overline{W}$ will remain low during consecutive data bus write cycles, such as when a double-byte store occurs. Refer to the example diagram of address and data demultiplexing.

2.4 Mode Selection

Operating modes are selected by a combination of logic levels applied to two input pins (MODA and MODB) during reset. The logic level present (at the rising edge of reset) on these inputs is reflected in bits in the HPRIO register. After reset, the operating mode may be changed according to the table contained in the following description of the HPRIO register.

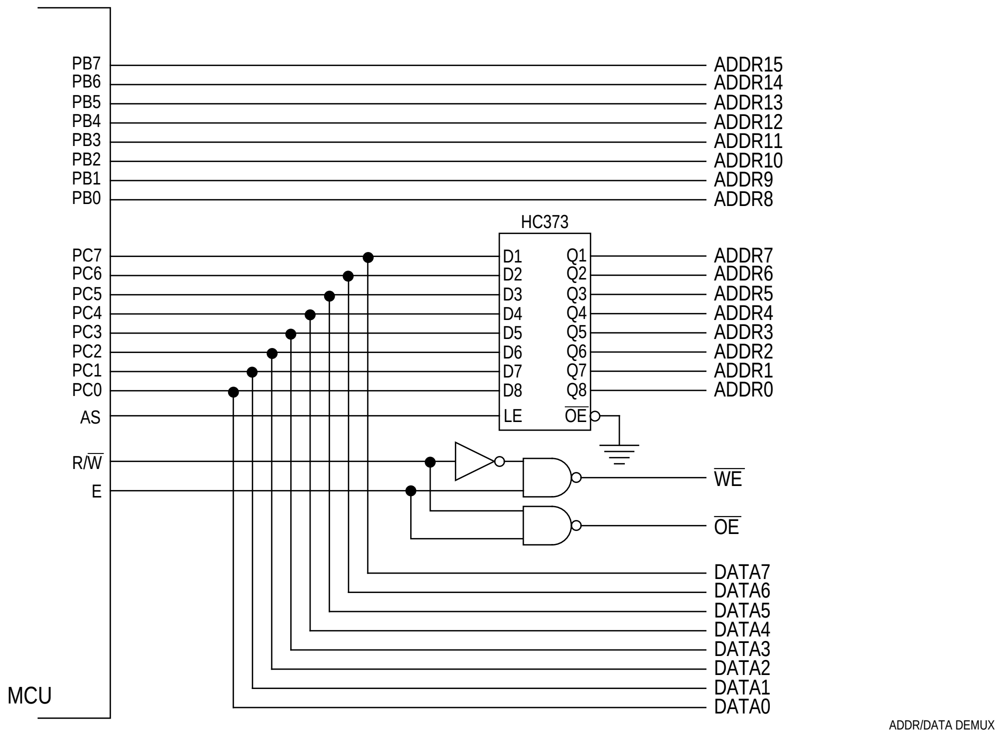

Figure 5 Address and Data Demultiplexing

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous **$003C**

	Bit 7	6	5	4	3	2	1	Bit 0	
	RBOOT*	SMOD*	MDA*	IRVNE*	PSEL3	PSEL2	PSEL1	PSEL0	
RESET:	0	0	1	0	0	1	0	1	Expanded
	1	1	0	0	0	1	0	1	Bootstrap
	0	1	1	1	0	1	0	1	Special Test

*The reset values of RBOOT, SMOD, MDA, and IRVNE depend on the mode selected at power up.

RBOOT — Read Bootstrap ROM

Valid only when SMOD is set (bootstrap or special test mode). Can only be written in special modes.

0 = Bootloader ROM disabled and not in map

1 = Bootloader ROM enabled and in map at $BE00–$BFFF

SMOD and MDA — Special Mode Select and Mode Select A

The initial value of SMOD is the **inverse** of the logic level present on the MODB pin at the rising edge of reset. The initial value of MDA equals the logic level present on the MODA pin at the rising edge of reset. These two bits can be read at any time. They can be written any time in special modes. MDA can only be written once in normal modes. SMOD cannot be set once it has been cleared.

Inputs		Mode	Latched at Reset	
MODB	MODA		SMOD	MDA
1	0	High-Impedance State ADDR/DATA (CPU held in reset)	0	0
1	1	Expanded	0	1
0	0	Bootstrap	1	0
0	1	Special Test	1	1

CAUTION

Unlike other M68HC11-family devices, the MC68HC11ED0 will not function in single-chip operating mode. If MODA is pulled low and MODB is pulled high at the rising edge of reset (the condition that causes most M68HC11 devices to enter single-chip mode) the CPU will remain in reset until the $\overline{\text{RESET}}$ pin is pulled low then released with appropriate logic levels applied to MODA and MODB.

IRVNE — Internal Read Visibility/Not E

IRVNE can be written once in any mode. In special test mode IRVNE is reset to one. In all other modes IRVNE is reset to zero.

In expanded and test modes, IRVNE determines whether internal read visibility (IRV) is on or off.

0 = No internal read visibility on external bus

1 = Data from internal reads is driven out of the external data bus.

In bootstrap mode, IRVNE determines whether the E clock drives out from the chip.

0 = E is driven out from the chip.

1 = E pin is driven low.

Mode	IRVNE Out of Reset	E Clock Out of Reset	IRV Out of Reset	IRVNE Affects Only	IRVNE Can Be Written
Expanded	0	On	Off	IRV	Once
Bootstrap	0	On	Off	E	Once
Special Test	1	On	On	IRV	Once

PSEL[3:0] — Priority Select Bits [3:0]

Refer to **5 Resets and Interrupts**.

3 On-Chip Memory

The MC68HC11ED0 contains 512 bytes of on-chip static RAM. There is no on-chip ROM. Since the MC68HC11ED0 is intended for expanded mode applications only, reset and interrupt vectors are not contained in on-chip resources. An external memory must provide these at locations $FFC0–$FFFF. Refer to the memory map diagram.

3.1 Memory Map and Register Block

The INIT register controls the location of the register block and RAM in the 64-Kbyte CPU address space. The 64-byte register block originates at $0000 after reset and can be placed at any four Kbyte boundary ($x000) by writing an appropriate value to the INIT register. Since the RAM also begins at $0000 after reset, 64 bytes are overlaid by the register block. Registers are a higher priority resource than RAM. Therefore, the RAM which is overlaid by registers is inaccessible. Either the registers or the RAM must be remapped in order to gain access to all 512 bytes of the RAM. Refer to the memory map diagram.

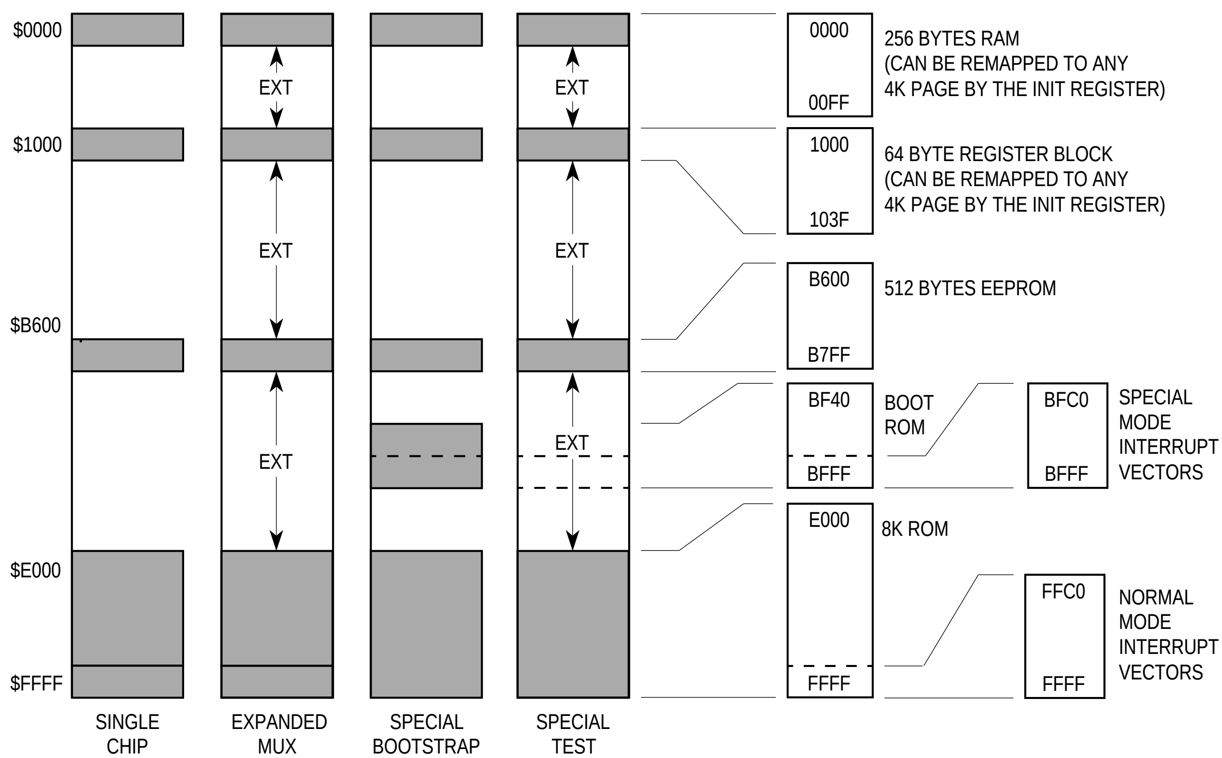

Figure 6 MC68HC11ED0 Memory Map

Table 2 MC68HC11ED0 Register and Control Bit Assignments

	Bit 7	6	5	4	3	2	1	Bit 0	
$0000	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PORTA
$0001									Reserved
$0002									Reserved
$0003									Reserved
$0004									Reserved
$0005									Reserved
$0006									Reserved
$0007									Reserved
$0008	0	0	PD5	PD4	PD3	PD2	PD1	PD0	PORTD
$0009	0	0	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	DDRD
$000A									Reserved
$000B	FOC1	FOC2	FOC3	FOC4	FOC5	0	0	0	CFORC
$000C	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	0	0	0	OC1M
$000D	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	0	0	0	OC1D
$000E	Bit 15	14	13	12	11	10	9	Bit 8	TCNT (High)
$000F	Bit 7	6	5	4	3	2	1	Bit 0	TCNT (Low)
$0010	Bit 15	14	13	12	11	10	9	Bit 8	TIC1 (High)
$0011	Bit 7	6	5	4	3	2	1	Bit 0	TIC1 (Low)
$0012	Bit 15	14	13	12	11	10	9	Bit 8	TIC2 (High)
$0013	Bit 7	6	5	4	3	2	1	Bit 0	TIC2 (Low)
$0014	Bit 15	14	13	12	11	10	9	Bit 8	TIC3 (High)
$0015	Bit 7	6	5	4	3	2	1	Bit 0	TIC3 (Low)
$0016	Bit 15	14	13	12	11	10	9	Bit 8	TOC1(High)
$0017	Bit 7	6	5	4	3	2	1	Bit 0	TOC1 (Low)
$0018	Bit 15	14	13	12	11	10	9	Bit 8	TOC2 (High)
$0019	Bit 7	6	5	4	3	2	1	Bit 0	TOC2 (Low)
$001A	Bit 15	14	13	12	11	10	9	Bit 8	TOC3 (High)
$001B	Bit 7	6	5	4	3	2	1	Bit 0	TOC3 (Low)
$001C	Bit 15	14	13	12	11	10	9	Bit 8	TOC4 (High)
$001D	Bit 7	6	5	4	3	2	1	Bit 0	TOC4 (Low)
$001E	Bit 15	14	13	12	11	10	9	Bit 8	TI4/O5 (High)
$001F	Bit 7	6	5	4	3	2	1	Bit 0	TI4/O5 (Low)
$0020	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5	TCTL1
$0021	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A	TCTL2
$0022	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I	TMSK1
$0023	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F	TFLG1
$0024	TOI	RTII	PAOVI	PAII	0	0	PR1	PR0	TMSK2
$0025	TOF	RTIF	PAOVF	PAIF	0	0	0	0	TFLG2
$0026	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0	PACTL
$0027	Bit 7	6	5	4	3	2	1	Bit 0	PACNT
$0028	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
$0029	SPIF	WCOL	0	MODF	0	0	0	0	SPSR
$002A	Bit 7	6	5	4	3	2	1	Bit 0	SPDR
$002B	TCLR	0	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0	BAUD
$002C	R8	T8	0	M	WAKE	0	0	0	SCCR1
$002D	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	SCCR2
$002E	TDRE	TC	RDRF	IDLE	OR	NF	FE	0	SCSR
$002F	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0	SCDR

Table 2 MC68HC11ED0 Register and Control Bit Assignments (Continued)

	Bit 7	6	5	4	3	2	1	Bit 0	
$0030									Reserved
$0031									Reserved
$0032									Reserved
$0033									Reserved
$0034									Reserved
$0035									Reserved
$0036									Reserved
$0037									Reserved
$0038									Reserved
$0039	0	0	IRQE	DLY	CME	0	CR1	CR0	OPTION
$003A	Bit 7	6	5	4	3	2	1	Bit 0	COPRST
$003B									Reserved
$003C	RBOOT	SMOD	MDA	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0	HPRIO
$003D	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0	INIT
$003E	—	—	—	—	—	—	—	—	TEST1*
$003F	0	0	0	0	0	NOCOP	0	0	CONFIG

*Factory Test Only

3.2 RAM

The MC68HC11ED0 has 512 bytes of on-chip static RAM. The RAM can be mapped to any four Kbyte boundary. Upon reset, the RAM is mapped at $0000–$01FF. The register block also begins at $0000 and overlaps the RAM space. Since registers have priority over RAM, this causes 64 bytes of RAM to be lost. However, the user can map either the RAM or the register block to any four Kbyte boundary ($x000) and access the full 512 bytes of RAM. Remapping is accomplished by writing appropriate values to the INIT register.

When power is removed from the MCU, RAM contents may be preserved using the MODB/V_{STBY} pin. A four volt nominal power source applied to this pin protects all 512 bytes of RAM.

INIT — RAM and Register Mapping **$003D**

	Bit 7	6	5	4	3	2	1	Bit 0
	RAM3	RAM2	RAM1	RAM0	REG3	REG2	REG1	REG0
RESET:	0	0	0	0	0	0	0	0

Can be written only once in first 64 cycles out of reset in normal modes or at any time in special modes.

RAM[3:0] — Internal RAM Map Position

These bits determine the upper four bits of the RAM address. At reset RAM is mapped to $0000 and includes the register block. Refer to the memory map diagram.

REG[3:0] — 128-Byte Register Block Map Position

These bits determine the upper four bits of the register space address. At reset registers are mapped to $0000 and overwrite the first 64 bytes of RAM. Refer to the memory map diagram.

4 Parallel Input/Output

The MC68HC11ED0 has up to 14 input/output lines. The address/data bus of this microcontroller is multiplexed and has no I/O ports associated with it. The following table is a summary of the configuration and features of each port.

Port	Input Pins	Output Pins	Bidirectional Pins	Shared Functions
Port A	3	3	2	Timer
Port D	—	—	6	SCI and SPI

NOTE

Do not confuse pin function with the electrical state of the pin at reset. All general-purpose I/O pins configured as inputs at reset are in a high-impedance state and the contents of port data registers is undefined. In port descriptions, a "U" indicates this condition. The pin function is mode dependent.

PORTA — Port A Data **$0000**

	Bit 7	6	5	4	3	2	1	Bit 0
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
RESET:	U	0	0	0	U	U	U	U
Alt. Pin Func.:	PAI	OC2	OC3	OC4	IC4/OC5	IC1	IC2	IC3
And/or:	OC1	OC1	OC1	OC1	OC1	—	—	—

NOTE

To enable PA3 as fourth input capture, set the I4/O5 bit in the PACTL register. Otherwise, PA3 is configured as a fifth output compare out of reset, with bit I4/O5 being cleared. If the DDRA3 bit in PACTL is set (configuring PA3 as an output), and IC4 is enabled, writes to PA3 cause edges on the pin to result in input captures. Writing to TI4/O5 has no effect when the TI4/O5 register is acting as IC4. PA7 drives the pulse accumulator input but also can be configured for general-purpose I/O or output compare. DDRA7 bit in PACTL register configures PA7 for either input or output. Note that even when PA7 is configured as an output, the pin still drives the pulse accumulator input.

PACTL — Pulse Accumulator Control **$0026**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

DDRA7 — Data Direction for Port A Bit 7

0 = Input only

1 = Output

PAEN — Pulse Accumulator System Enable

Refer to **7 Pulse Accumulator**.

PAMOD — Pulse Accumulator Mode

Refer to **7 Pulse Accumulator**.

PEDGE — Pulse Accumulator Edge Control
Refer to **7 Pulse Accumulator**.

DDRA3 — Data Direction for Port A Bit 3
Overridden if an output compare function is configured to control the PA3 pin.
0 = Input
1 = Output

I4/O5 — Input Capture 4/Output Compare 5
Refer to **6 Main Timer**.

RTR[1:0] — Real-Time Interrupt (RTI) Rate
Refer to **7 Pulse Accumulator**.

PORTD — Port D Data **$0008**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	PD5	PD4	PD3	PD2	PD1	PD0
RESET:	0	0	U	U	U	U	U	U
Alt. Pin Func.:	—	—	$\overline{SS}$	SCK	MOSI	MISO	TxD	RxD

DDRD — Data Direction Register for Port D **$0009**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
RESET:	0	0	0	0	0	0	0	0

Bits [7:6] — Not implemented
Always read zero

DDD[5:0] — Data Direction for Port D
0 = Input
1 = Output

NOTE

When the SPI system is in slave mode, DDD5 has no meaning nor effect. When the SPI system is in master mode, DDD5 determines whether bit 5 of PORTD is an error detect input (DDD5 = 0) or a general-purpose output (DDD5 = 1). If the SPI system is enabled and expects any of bits [4:2] to be an input that bit will be an input regardless of the state of the associated DDR bit. If any of bits [4:2] are expected to be outputs that bit will be an output **only** if the associated DDR bit is set.

5 Resets and Interrupts

The MC68HC11ED0 has three reset vectors and 18 interrupt vectors. The reset vectors are as follows:

- $\overline{\text{RESET}}$, or Power-On Reset
- Clock Monitor Fail
- COP Failure

The 18 interrupt vectors service 22 interrupt sources (three nonmaskable, 19 maskable). The three non-maskable interrupt sources are as follows:

- $\overline{\text{XIRQ}}$ Pin (X-Bit Interrupt)
- Illegal Opcode Trap
- Software Interrupt

On-chip peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the condition code register (CCR) is clear. Maskable interrupts are prioritized according to a default arrangement; however, any one source can be elevated to the highest maskable priority position by a software-accessible control register (HPRIO). The HPRIO register can be written at any time, provided bit I in the CCR is set.

Nineteen interrupt sources in the MC68HC11ED0 are subject to masking by the global interrupt mask bit (bit I in the CCR). In addition to the global bit I, all of these sources, except the external interrupt ($\overline{\text{IRQ}}$) pin, are controlled by local enable bits in control registers. Most interrupt sources in M68HC11 devices have separate interrupt vectors; therefore, there is usually no need for software to poll control registers to determine the cause of an interrupt.

For some interrupt sources, such as the SCI interrupts, the flags are automatically cleared during the normal course of responding to the interrupt requests. For example, the RDRF flag in the SCI system is cleared by the automatic clearing mechanism invoked by a read of the SCI status register while RDRF is set, followed by a read of the SCI data register. The normal response to an RDRF interrupt request would be to read the SCI status register to check for receive errors, then to read the received data from the SCI data register. These two steps satisfy the automatic clearing mechanism without requiring any special instructions.

Refer to Table 3 for interrupt and reset vector assignments.

Table 3 Interrupt and Reset Vector Assignments

Vector Address	Interrupt Source	CCR Mask Bit	Local Mask	Priority (1 = High)
FFC0, C1 — FFD4, D5	Reserved	—	—	—
FFD6, D7	SCI Serial System	I		
	• SCI Receive Data Register Full		RIE	19
	• SCI Receiver Overrun		RIE	20
	• SCI Transmit Data Register Empty		TIE	21
	• SCI Transmit Complete		TCIE	22
	• SCI Idle Line Detect		ILIE	23
FFD8, D9	SPI Serial Transfer Complete	I	SPIE	18
FFDA, DB	Pulse Accumulator Input Edge	I	PAII	17
FFDC, DD	Pulse Accumulator Overflow	I	PAOVI	16
FFDE, DF	Timer Overflow	I	TOI	15
FFE0, E1	Timer Input Capture 4/Output Compare 5	I	I4/O5I	14
FFE2, E3	Timer Output Compare 4	I	OC4I	13
FFE4, E5	Timer Output Compare 3	I	OC3I	12
FFE6, E7	Timer Output Compare 2	I	OC2I	11
FFE8, E9	Timer Output Compare 1	I	OC1I	10
FFEA, EB	Timer Input Capture 3	I	IC3I	9
FFEC, ED	Timer Input Capture 2	I	IC2I	8
FFEE, EF	Timer Input Capture 1	I	IC1I	7
FFF0, F1	Real Time Interrupt	I	RTII	6
FFF2, F3	$\overline{\text{IRQ}}$	I	None	5
FFF4, F5	$\overline{\text{XIRQ}}$ Pin	X	None	4
FFF6, F7	Software Interrupt	None	None	*
FFF8, F9	Illegal Opcode Trap	None	None	*
FFFA, FB	COP Failure	None	NOCOP	3
FFFC, FD	Clock Monitor Fail	None	CME	2
FFFE, FF	$\overline{\text{RESET}}$	None	None	1

* Same level as an instruction

OPTION — System Configuration Options **$0039**

	Bit 7	6	5	4	3	2	1	Bit 0
	—	—	IRQE*	DLY*	CME	—	CR1*	CR0*
RESET:	0	0	0	1	0	0	0	0

*Can be written only once in first 64 cycles out of reset in normal modes, or at any time in special modes.

Bits [7:6] — Not implemented
Always read zero

IRQE — $\overline{\text{IRQ}}$ Select Edge Sensitive Only
0 = Low level recognition
1 = Falling edge recognition

DLY — Enable Oscillator Start-Up Delay on Exit from STOP

0 = No stabilization delay on exit from STOP
1 = Stabilization delay enabled on exit from STOP

CME — Clock Monitor Enable

0 = Clock monitor disabled; slow clocks can be used
1 = Slow or stopped clocks cause clock failure reset

Bit 2 — Not implemented

Always reads zero

CR[1:0] — COP Timer Rate Select

Refer to NOCOP bit in CONFIG register.

Table 4 COP Timer Rate Select (Time-out Period Length)

CR[1:0]	Rate Selected	XTAL = 4.0 MHz Time-out –0 ms, +32.8 ms	XTAL = 8.0 MHz Time-out –0 ms, +16.4 ms	XTAL = 12.0 MHz Time-out –0 ms, +10.9 ms
0 0	2^{15}/E	32.768 ms	16.384 ms	10.923 ms
0 1	2^{17}/E	131.07 ms	65.536 ms	43.691 ms
1 0	2^{19}/E	524.29 ms	262.14 ms	174.76 ms
1 1	2^{21}/E	2.1 s	1.049 s	699.05 ms
	E =	1.0 MHz	2.0 MHz	3.0 MHz

COPRST — Arm/Reset COP Timer Circuitry **$003A**

	Bit 7	6	5	4	3	2	1	Bit 0
	7	6	5	4	3	2	1	0
RESET:	0	0	0	0	0	0	0	0

Write $55 to COPRST to arm COP watchdog clearing mechanism. Write $AA to COPRST to reset COP watchdog. Refer to NOCOP bit in CONFIG register.

5.1 Configuration Control Register (CONFIG)

In many M68HC11 devices the CONFIG register is used to define various system functions. The CONFIG register in the MC68HC11ED0 controls only one MCU function. The NOCOP bit disables the COP watchdog circuit when it is set. Refer to Table 4.

CONFIG — System Configuration Register **$003F**

	Bit 7	6	5	4	3	2	1	Bit 0	
	—	—	—	—	—	NOCOP	—	—	
RESET:	0	0	0	0	0	0	0	0	Expanded Mode
	0	0	0	0	0	1	0	0	Special Test
	0	0	0	0	0	1	0	0	Bootstrap

Must be written during the first 64 cycles after reset in normal modes (SMOD = 0) or at any time in special modes (SMOD = 1).

Bits [7:3] — Not implemented

Always read zero

NOCOP — COP System Disable
Resets to programmed value
0 = COP enabled (forces reset on time-out)
1 = COP disabled (does not force reset on time-out)

Bits [1:0] — Not implemented
Always read zero

HPRIO — Highest Priority I-Bit Interrupt and Miscellaneous **$003C**

	Bit 7	6	5	4	3	2	1	Bit 0
	RBOOT*	SMOD*	MDA*	IRVNE	PSEL3	PSEL2	PSEL1	PSEL0
RESET:	—	—	—	—	0	1	0	1

*RBOOT, SMOD, and MDA reset depend on power-up initialization mode and can only be written in special mode.

RBOOT — Read Bootstrap ROM
Refer to **2 Operating Modes**.

SMOD — Special Mode Select
Refer to **2 Operating Modes**.

MDA — Mode Select A
Refer to **2 Operating Modes**.

IRVNE — Internal Read Visibility/Not E
Refer to **2 Operating Modes**.

PSEL[3:0] — Priority Select Bits [3:0]
Can be written only while the I bit in the CCR is set (interrupts disabled). These bits select one interrupt source to be elevated above all other I-bit related sources.

PSEL[3:0]				**Interrupt Source Promoted**
0	0	0	0	Timer Overflow
0	0	0	1	Pulse Accumulator Overflow
0	0	1	0	Pulse Accumulator Input Edge
0	0	1	1	SPI Serial Transfer Complete
0	1	0	0	SCI Serial System
0	1	0	1	Reserved (Default to $\overline{IRQ}$)
0	1	1	0	$\overline{IRQ}$
0	1	1	1	Real-Time Interrupt
1	0	0	0	Timer Input Capture 1
1	0	0	1	Timer Input Capture 2
1	0	1	0	Timer Input Capture 3
1	0	1	1	Timer Output Compare 1
1	1	0	0	Timer Output Compare 2
1	1	0	1	Timer Output Compare 3
1	1	1	0	Timer Output Compare 4
1	1	1	1	Timer Output Compare 5/Input Capture 4

6 Main Timer

The timing system is based on a free-running 16-bit counter with a four-stage programmable prescaler. A timer overflow function allows software to extend the system's timing capability beyond the counter's 16-bit range.

The timer has three channels for input capture, four channels for output compare, and one channel that can be configured as a fourth input capture or a fifth output compare. In addition, the timing system includes pulse accumulator and real-time interrupt (RTI) functions, as well as a clock monitor function, which can be used to detect clock failures that are not detected by the COP.

Refer to **7 Pulse Accumulator** for further information about these functions. Refer to the following table for a summary of the crystal-related frequencies and periods.

Table 5 Timer Summary

Control Bits	Common System Frequencies			Definition
	4.0 MHz	**8.0 MHz**	**12.0 MHz**	**XTAL**
	1.0 MHz	**2.0 MHz**	**3.0 MHz**	**E**
PR[1:0]	**Main Timer Count Rates (Period Length)**			
0 0 1 count — overflow —	1000 ns 65.536 ms	500 ns 32.768 ms	333 ns 21.845 ms	1/E 2^{16}/E
0 1 1 count — overflow —	4.0 µs 262.14 ms	2.0 µs 131.07 ms	1.333 µs 87.381 ms	4/E 2^{18}/E
1 0 1 count — overflow —	8.0 µs 524.28 ms	4.0 µs 262.14 ms	2.667 µs 174.76 ms	8/E 2^{19}/E
1 1 1 count — overflow —	16.0 µs 1.049 s	8.0 µs 524.29 ms	5.333 µs 349.52 ms	16/E 2^{20}/E
RTR[1:0]	**Periodic (RTI) Interrupt Rates (Period Length)**			
0 0 0 1 1 0 1 1	8.192 ms 16.384 ms 32.768 ms 65.536 ms	4.096 ms 8.192 ms 16.384 ms 32.768 ms	2.731 ms 5.461 ms 10.923 ms 21.845 ms	2^{13}/E 2^{14}/E 2^{15}/E 2^{16}/E
CR[1:0]	**COP Watchdog Timeout Rates (Period Length)**			
0 0 0 1 1 0 1 1	32.768 ms 131.072 ms 524.288 ms 2.098 s	16.384 ms 65.536 ms 262.14 ms 1.049 s	10.923 ms 43.691 ms 174.76 ms 699.05 ms	2^{15}/E 2^{17}/E 2^{19}/E 2^{21}/E
Timeout Tolerance (– 0 ms/+...)	32.8 ms	16.4 ms	10.9 ms	2^{15}/E

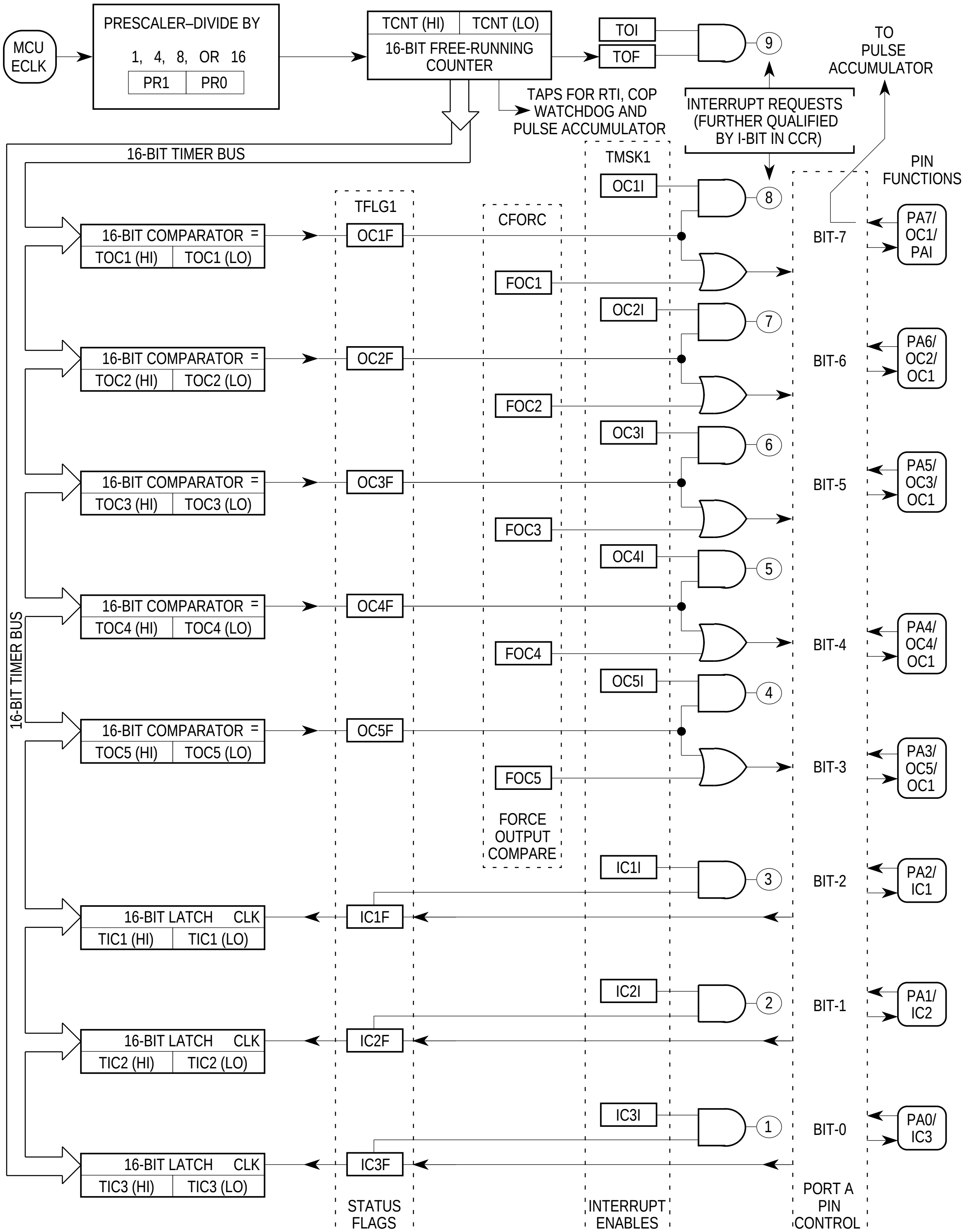

Figure 7 Timer Block Diagram

CFORC — Timer Compare Force **$000B**

	Bit 7	6	5	4	3	2	1	Bit 0
	FOC1	FOC2	FOC3	FOC4	FOC5	—	—	—
RESET:	0	0	0	0	0	0	0	0

FOC[5:1] — Force Output Compare
Write ones to force compare(s)
0 = Not affected
1 = Output x action occurs

Bits [2:0] — Not implemented
Always read zero

OC1M — Output Compare 1 Mask **$000C**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1M7	OC1M6	OC1M5	OC1M4	OC1M3	—	—	—
RESET:	0	0	0	0	0	0	0	0

Set bit(s) to enable OC1 to control corresponding pin(s) of port A

Bits [2:0] — Not implemented
Always read zero

OC1D — Output Compare 1 Data **$000D**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1D7	OC1D6	OC1D5	OC1D4	OC1D3	—	—	—
RESET:	0	0	0	0	0	0	0	0

If OC1Mx is set, data in OC1Dx is output to port A bit x on successful OC1 compares.

Bits [2:0] — Not implemented
Always read zero

TCNT — Timer Count **$000E–$000F**

$000E	Bit 15	14	13	12	11	10	9	Bit 8	High	**TCNT**
$000F	Bit 7	6	5	4	3	2	1	Bit 0	Low	

TCNT resets to $0000. In normal modes, TCNT is read-only.

TIC1–TIC3 — Timer Input Capture **$0010–$0015**

$0010	Bit 15	14	13	12	11	10	9	Bit 8	High **TIC1**
$0011	Bit 7	6	5	4	3	2	1	Bit 0	Low
$0012	Bit 15	14	13	12	11	10	9	Bit 8	High **TIC2**
$0013	Bit 7	6	5	4	3	2	1	Bit 0	Low
$0014	Bit 15	14	13	12	11	10	9	Bit 8	High **TIC3**
$0015	Bit 7	6	5	4	3	2	1	Bit 0	Low

TICx not affected by reset.

TOC1–TOC4 — Timer Output Compare **$0016–$001D**

$0016	Bit 15	14	13	12	11	10	9	Bit 8	High **TOC1**
$0017	Bit 7	6	5	4	3	2	1	Bit 0	Low
$0018	Bit 15	14	13	12	11	10	9	Bit 8	High **TOC2**
$0019	Bit 7	6	5	4	3	2	1	Bit 0	Low
$001A	Bit 15	14	13	12	11	10	9	Bit 8	High **TOC3**
$001B	Bit 7	6	5	4	3	2	1	Bit 0	Low
$001C	Bit 15	14	13	12	11	10	9	Bit 8	High **TOC4**
$001D	Bit 7	6	5	4	3	2	1	Bit 0	Low

All TOCx register pairs reset to ones ($FFFF).

TI4/O5 — Timer Input Capture 4/Output Compare 5 **$001E–$001F**

$001E	Bit 15	14	13	12	11	10	9	Bit 8	High
$001F	Bit 7	6	5	4	3	2	1	Bit 0	Low

This is a shared register and is either input capture 4 or output compare 5 depending on the state of bit I4/O5 in PACTL. Writes to TI4/O5 have no effect when this register is configured as input capture 4. The TI4/O5 register pair resets to ones ($FFFF).

TCTL1 — Timer Control 1 **$0020**

	Bit 7	6	5	4	3	2	1	Bit 0
	OM2	OL2	OM3	OL3	OM4	OL4	OM5	OL5
RESET:	0	0	0	0	0	0	0	0

OM[5:2] — Output Mode

OL[5:2] — Output Level

OMx	OLx	Action Taken on Successful Compare
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

TCTL2 — Timer Control 2 **$0021**

	Bit 7	6	5	4	3	2	1	Bit 0
	EDG4B	EDG4A	EDG1B	EDG1A	EDG2B	EDG2A	EDG3B	EDG3A
RESET:	0	0	0	0	0	0	0	0

EDGxB	EDGxA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge

TMSK1 — Timer Interrupt Mask 1 **$0022**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1I	OC2I	OC3I	OC4I	I4/O5I	IC1I	IC2I	IC3I
RESET:	0	0	0	0	0	0	0	0

OC1I –OC4I — Output Compare x Interrupt Enable

If the OCxF flag bit is set while the OCxI enable bit is set, a hardware interrupt sequence is requested.

I4/O5I — Input Capture 4 or Output Compare 5 Interrupt Enable

When I4/O5 in PACTL is one, I4/O5I is the input capture 4 interrupt bit. When I4/O5 in PACTL is zero, I4/O5I is the output compare 5 interrupt control bit.

If the ICxF flag bit is set while the ICxI enable bit is set, a hardware interrupt sequence is requested.

NOTE

Control bits in TMSK1 correspond bit for bit with flag bits in TFLG1. Ones in TMSK1 enable the corresponding interrupt sources.

TFLG1 — Timer Interrupt Flag 1 **$0023**

	Bit 7	6	5	4	3	2	1	Bit 0
	OC1F	OC2F	OC3F	OC4F	I4/O5F	IC1F	IC2F	IC3F
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

OC1F–OC4F — Output Compare x Flag

Set each time the counter matches output compare x value

I4/O5F — Input Capture 4/Output Compare 5 Flag

Set by IC4 or OC5, depending on which function was enabled by I4/O5 of PACTL

IC1F–IC3F — Input Capture x Flag

Set each time a selected active edge is detected on the ICx input line

TMSK2 — Timer Interrupt Mask 2 **$0024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	—	—	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt Enable

0 = Timer Overflow Interrupt Disabled

1 = Timer Overflow Interrupt Enabled

RTII — Real-Time Interrupt Enable

0 = RTIF interrupts disabled

1 = Interrupt requested when RTIF is set to one.

PAOVI — Pulse Accumulator Overflow Interrupt Enable

Refer to **7 Pulse Accumulator**.

PAII — Pulse Accumulator Interrupt Enable

Refer to **7 Pulse Accumulator**.

Bits [3:2] — Not implemented
Always read zero

PR[1:0] — Timer Prescaler Select
In normal modes, PR1 and PR0 can only be written once, and the write must occur within 64 cycles after reset. Refer to Table 5 for specific timing values.

PR[1:0]	Prescaler
0 0	÷ 1
0 1	÷ 4
1 0	÷ 8
1 1	÷ 16

NOTE

Control bits [7:4] in TMSK2 correspond bit for bit with flag bits [7:4] in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

TFLG2 — Timer Interrupt Flag 2 **$0025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	—	—	—	—
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Flag
Set when TCNT changes from $FFFF to $0000

RTIF — Real-Time (Periodic) Interrupt Flag
Set periodically. Refer to RTR[1:0] bits in PACTL register.

PAOVF — Pulse Accumulator Overflow Flag
Refer to **7 Pulse Accumulator**.

PAIF — Pulse Accumulator Input Edge Flag
Refer to **7 Pulse Accumulator**.

Bits [3:0] — Not implemented
Always read zero

PACTL — Pulse Accumulator Control **$0026**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

DDRA7 — Data Direction for Port A Bit 7
Refer to **4 Parallel Input/Output**.

PAEN — Pulse Accumulator System Enable
Refer to **7 Pulse Accumulator**.

PAMOD — Pulse Accumulator Mode
Refer to **7 Pulse Accumulator**.

PEDGE — Pulse Accumulator Edge Control
Refer to **7 Pulse Accumulator**.

DDRA3 — Data Direction for Port A Bit 3
Refer to **4 Parallel Input/Output**.

I4/O5 — Input Capture 4/Output Compare 5
Configure TI4/O5 for input capture or output compare
0 = OC5 enabled
1 = IC4 enabled

RTR[1:0] — Real-Time Interrupt (RTI) Rate
Refer to **7 Pulse Accumulator**.

7 Pulse Accumulator

The MC68HC11ED0 has an 8-bit counter that can be configured as a simple event counter or for gated time accumulation. The counter can be read or written at any time.

The port A bit 7 I/O pin can be configured to act as a clock in event counting mode, or as a gate signal to enable a free-running clock (E divided by 64) to the 8-bit counter in gated time accumulation mode.

Table 6 Pulse Accumulator Timing

		Common XTAL Frequencies		
		4.0 MHz	**8.0 MHz**	**12.0 MHz**
CPU Clock	(E)	1.0 MHz	2.0 MHz	3.0 MHz
Cycle Time	(1/E)	1000 ns	500 ns	333 ns
Pulse Accumulator (Gated Mode)				
1 Count —	(2^6/E)	64.0 µs	32.0 µs	21.330 µs
Overflow —	(2^{14}/E)	16.384 ms	8.192 ms	5.491 ms

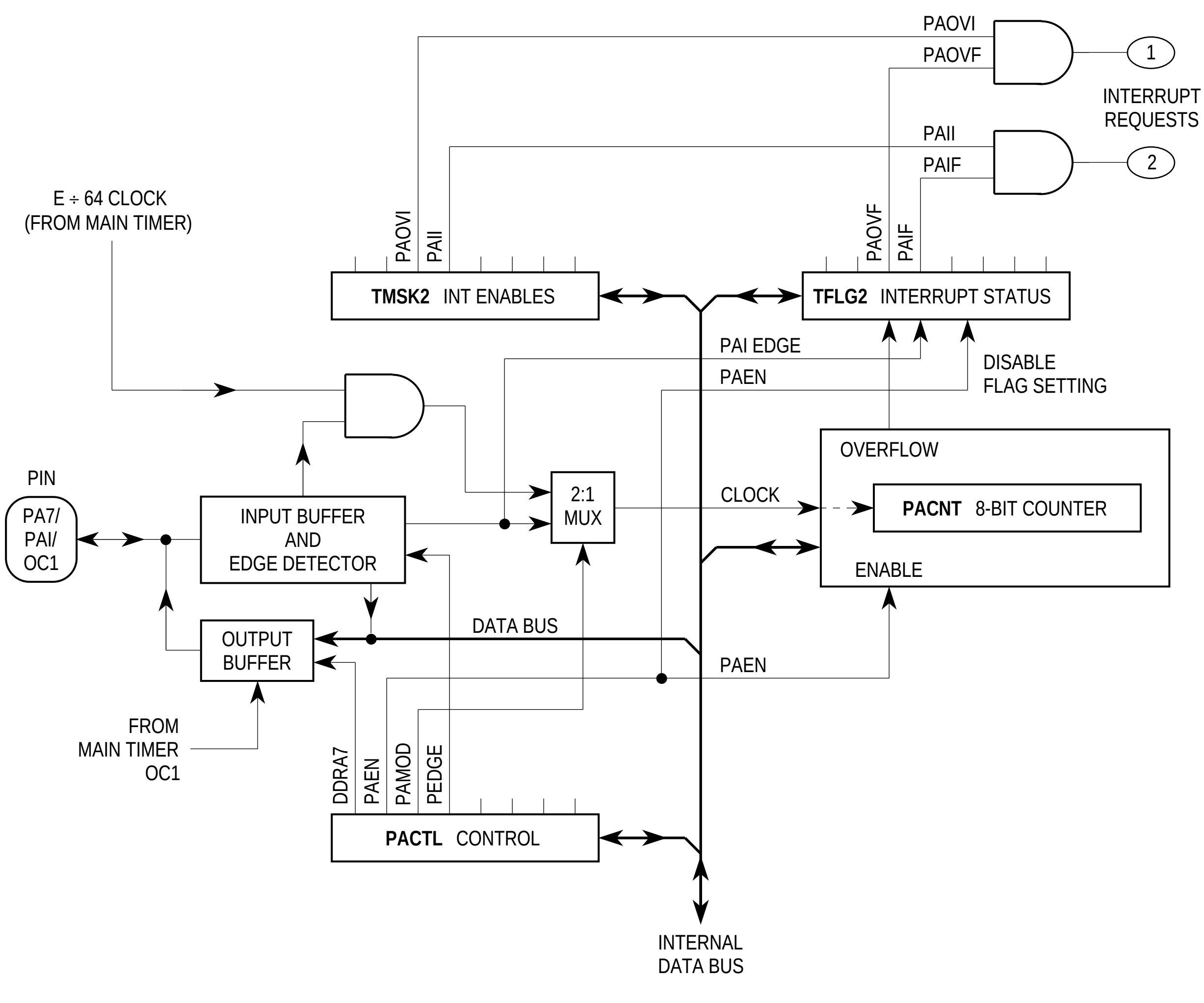

Figure 8 Pulse Accumulator System Block Diagram

TMSK2 — Timer Interrupt Mask 2 **$0024**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOI	RTII	PAOVI	PAII	—	—	PR1	PR0
RESET:	0	0	0	0	0	0	0	0

TOI — Timer Overflow Interrupt Enable
Refer to **6 Main Timer**.

RTII — Real-Time Interrupt Enable
Refer to **6 Main Timer**.

PAOVI — Pulse Accumulator Overflow Interrupt Enable
0 = Pulse accumulator overflow interrupt disabled
1 = Pulse accumulator overflow interrupt enabled

PAII — Pulse Accumulator Input Interrupt Enable
0 = Pulse accumulator input interrupt disabled
1 = Pulse accumulator input interrupt enabled if PAIF bit in TFLG2 register is set

Bits [3:2] — Not implemented
Always read zero

PR[1:0] — Timer Prescaler Select
Refer to **6 Main Timer**.

NOTE

Control bits [7:4] in TMSK2 correspond bit for bit with flag bits [7:4] in TFLG2. Ones in TMSK2 enable the corresponding interrupt sources.

TFLG2 — Timer Interrupt Flag 2 **$0025**

	Bit 7	6	5	4	3	2	1	Bit 0
	TOF	RTIF	PAOVF	PAIF	—	—	—	—
RESET:	0	0	0	0	0	0	0	0

Clear flags by writing a one to the corresponding bit position(s).

TOF — Timer Overflow Enable
Refer to **6 Main Timer**.

RTIF — Real-Time Interrupt Flag
Refer to **6 Main Timer**.

PAOVF — Pulse Accumulator Overflow Flag
Set when PACNT changes from $FF to $00

PAIF — Pulse Accumulator Input Edge Flag
Set each time a selected active edge is detected on the PAI input line

Bits [3:0] — Not implemented
Always read zero

PACTL — Pulse Accumulator Control **$0026**

	Bit 7	6	5	4	3	2	1	Bit 0
	DDRA7	PAEN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
RESET:	0	0	0	0	0	0	0	0

DDRA7 — Data Direction for Port A Bit 7

Refer to **4 Parallel Input/Output**.

PAEN — Pulse Accumulator System Enable

0 = Pulse Accumulator disabled

1 = Pulse Accumulator enabled

PAMOD — Pulse Accumulator Mode

0 = Event counter

1 = Gated time accumulation

PEDGE — Pulse Accumulator Edge Control

0 = In event mode, falling edges increment counter. In gated accumulation mode, high level enables accumulator and falling edge sets PAIF.

1 = In event mode, rising edges increment counter. In gated accumulation mode, low level enables accumulator and rising edge sets PAIF.

DDRA3 — Data Direction for Port A Bit 3

Refer to **4 Parallel Input/Output**.

I4/O5 — Input Capture 4/Output Compare 5

Refer to **6 Main Timer**.

RTR[1:0] — Real-Time Interrupt Rate

These two bits select the rate for periodic interrupts. Refer to the following tables.

Table 7 Real-Time Interrupt Rates (Period Length)

RTR[1:0]	Period Length	Period Length		
		Selected	E = 1.0 MHz	E = 2.0 MHz
0 0	$2^{13} \div E$	8.19 ms	4.096 ms	2.731 ms
0 1	$2^{14} \div E$	16.38 ms	8.192 ms	5.461 ms
1 0	$2^{15} \div E$	32.77 ms	16.384 ms	10.923 ms
1 1	$2^{16} \div E$	65.54 ms	32.768 ms	21.845 ms

Table 8 Real-Time Interrupt Rates (Frequency)

RTR[1:0]		Frequency		
		Rate Selected	E = 1.0 MHz	E = 2.0 MHz
0 0	$E \div 2^{13}$	122.070 Hz	244.141 Hz	366.211 Hz
0 1	$E \div 2^{14}$	61.035 Hz	122.070 Hz	183.105 Hz
1 0	$E \div 2^{15}$	30.518 Hz	61.035 Hz	91.553 Hz
1 1	$E \div 2^{16}$	15.259 Hz	30.518 Hz	45.776 Hz

PACNT — Pulse Accumulator Counter **$0027**

	Bit 7	6	5	4	3	2	1	Bit 0
	Bit 7	6	5	4	3	2	1	Bit 0
RESET:	U	U	U	U	U	U	U	U

Can be read and written.

8 Serial Communications Interface

The SCI is a universal asynchronous receiver transmitter (UART) serial communications interface, one of two independent serial I/O subsystems in the MC68HC11ED0. It has a standard nonreturn to zero (NRZ) format (one start bit, eight or nine data bits and one stop bit) and several baud rates available. The SCI transmitter and receiver are independent, but use the same data format and bit rate.

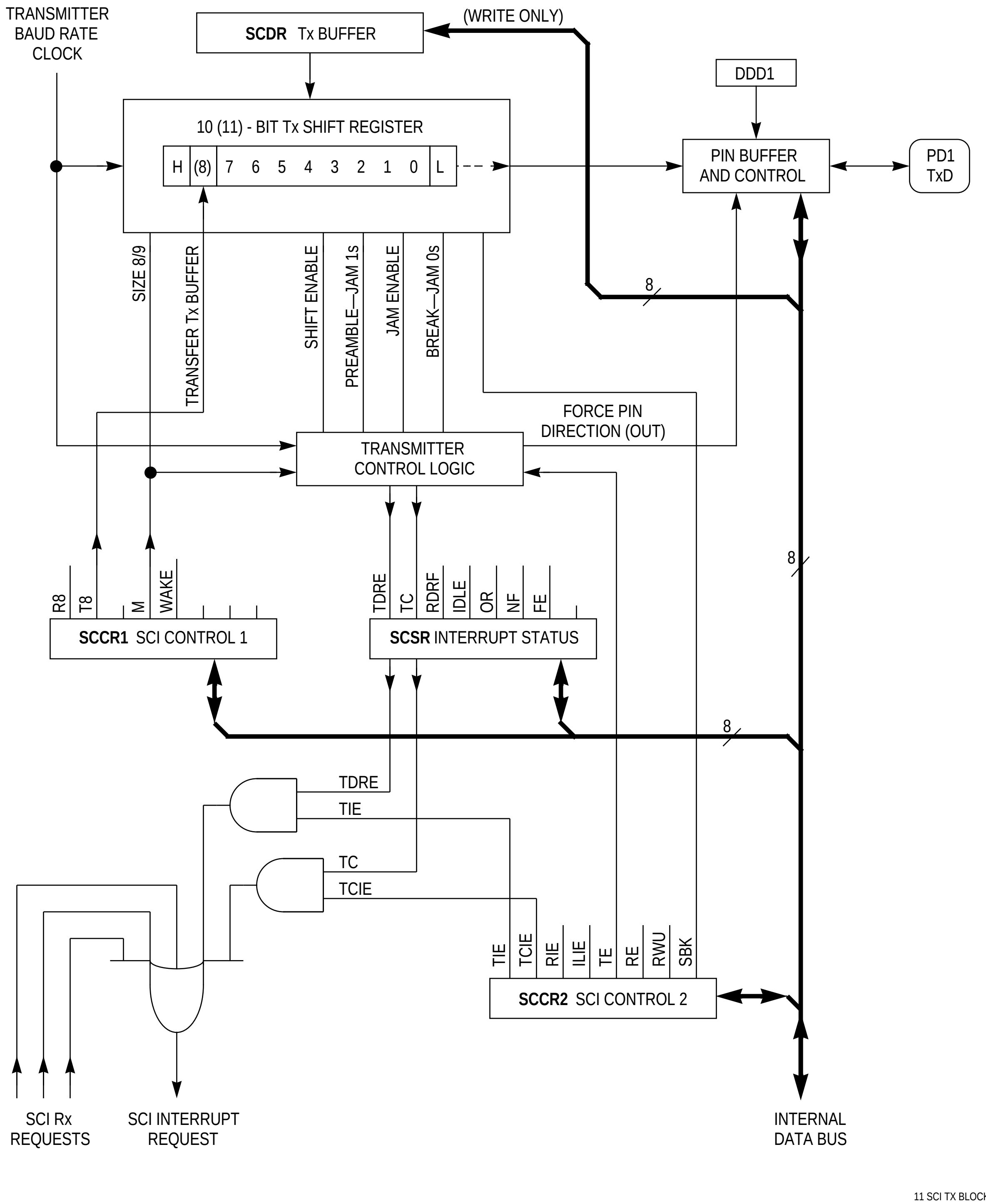

Figure 9 SCI Transmitter Block Diagram

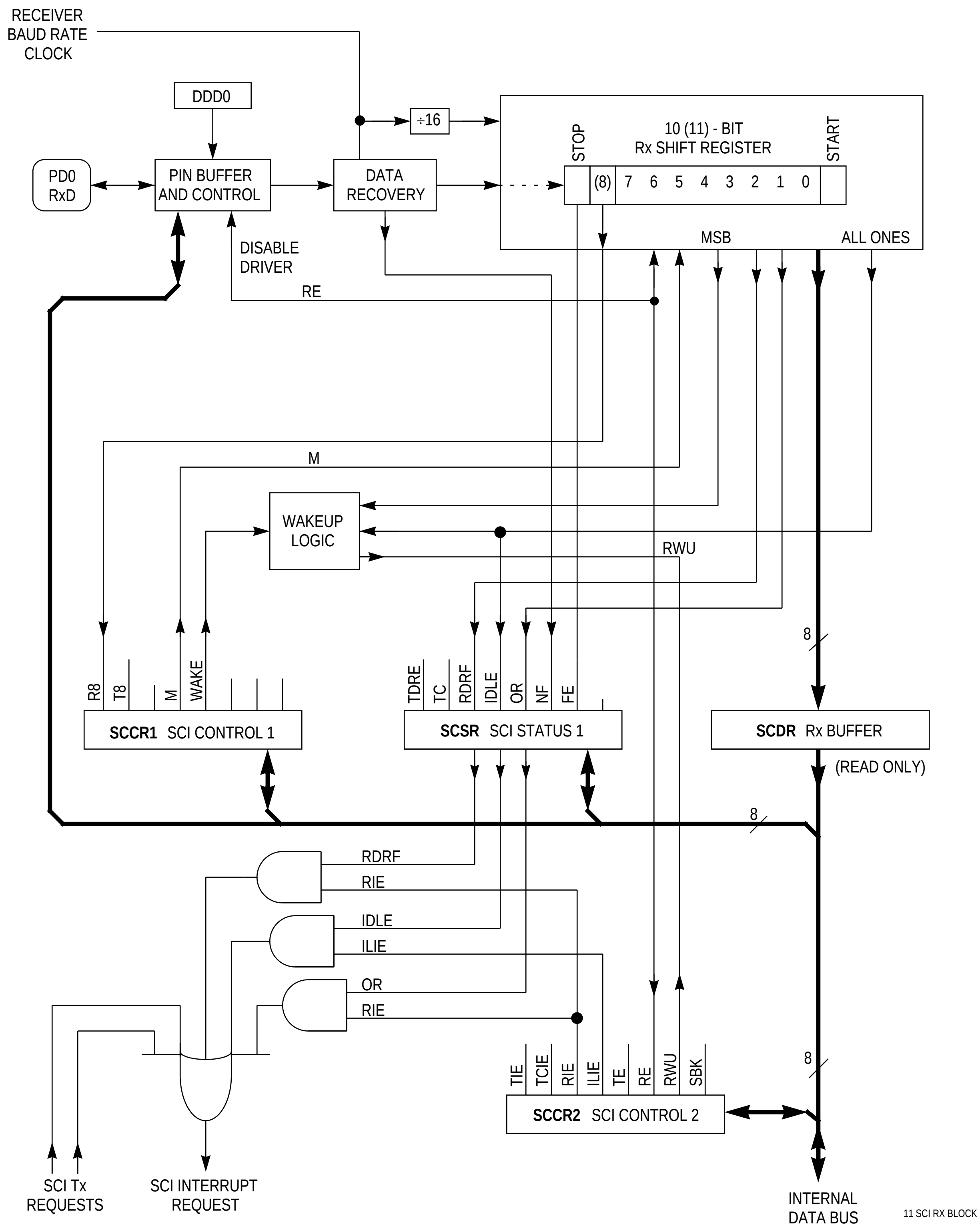

Figure 10 SCI Receiver Block Diagram

BAUD — Baud Rate **$002B**

	Bit 7	6	5	4	3	2	1	Bit 0
	TCLR	—	SCP1	SCP0	RCKB	SCR2	SCR1	SCR0
RESET:	0	0	0	0	0	U	U	U

TCLR — Clear Baud Rate Counters

Can only be set in test modes.

1 = Clear baud rate counter chain for testing purposes.

0 = Normal SCI operation

SCP[1:0] — SCI Baud Rate Prescaler Selects

Shaded boxes contain the prescaler rates used in the Baud Rate table (refer to SCR[2:0]). Refer to the SCI Baud Rate Clock Diagram.

SCP[1:0]	Divide E Clock By	Crystal Frequency in MHz		
		4.0 MHz (Baud)	8.0 MHz (Baud)	12.0 MHz (Baud)
0 0	1	62.50 K	125.0 K	187.5 K
0 1	3	20.83 K	41.67 K	62.5 K
1 0	4	15.625 K	31.25 K	46.88 K
1 1	13	4800	9600	14.4 K

RCKB — SCI Baud Rate Clock Check

Can only be set in test modes.

1 = Exclusive-OR of the RT clock driven out TxD pin for testing purposes.

0 = Normal SCI operation

SCR[2:0] — SCI Baud Rate Selects

Selects receiver and transmitter bit rate based on output from baud rate prescaler stage. Shaded boxes contain the prescaler output rates shown in the preceding table. Refer to the SCI Baud Rate Clock Diagram.

SCR[2:0]	Divide Prescaler By	Baud Rate (Prescaler Output from Previous Table)		
		4800	9600	14.4 K
0 0 0	1	4800	9600	14.4
0 0 1	2	2400	4800	7200
0 1 0	4	1200	2400	3600
0 1 1	8	600	1200	1800
1 0 0	16	300	600	1200
1 0 1	32	150	300	450
1 1 0	64	75	150	225
1 1 1	128	37.5	75	112.5

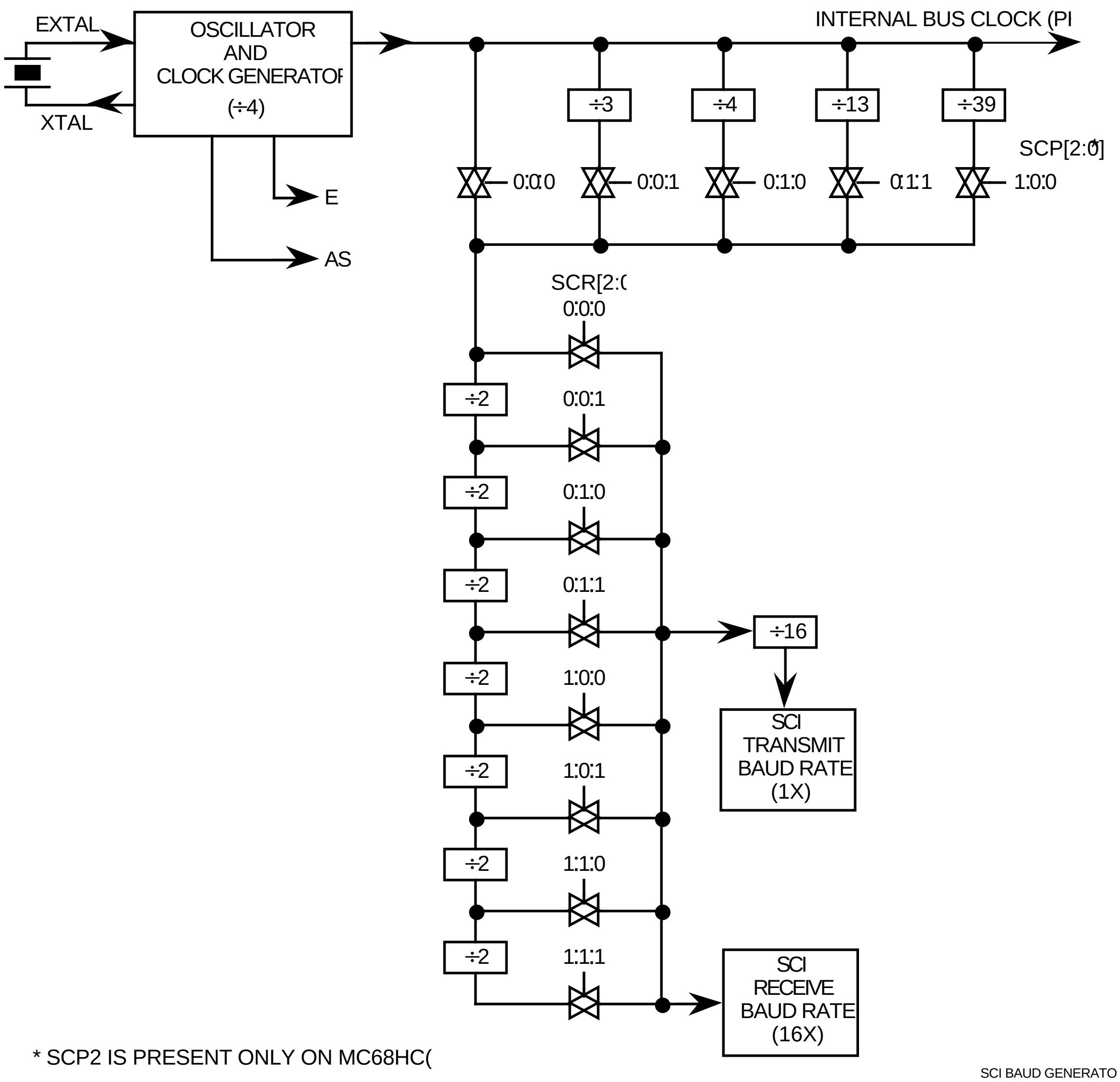

Figure 11 SCI Baud Rate Clock Diagram

SCCR1 — SCI Control 1 **$002C**

	Bit 7	6	5	4	3	2	1	Bit 0
	R8	T8	—	M	WAKE	—	—	—
RESET:	0	0	0	0	0	0	0	0

R8 — Receive Data Bit 8
If M bit is set, R8 stores ninth bit in receive data character.

T8 — Transmit Data bit 8
If M bit is set, T8 stores ninth bit in transmit data character.

Bit 5 — Not implemented
Always reads zero

M — Mode (Select Character Format)
0 = Start bit, 8 data bits, 1 stop bit
1 = Start bit, 9 data bits, 1 stop bit

WAKE — Wakeup by Address Mark/Idle
0 = Wakeup by IDLE line recognition
1 = Wakeup by address mark (most significant data bit set)

Bits [2:0] — Not implemented
Always read zero.

SCCR2 — SCI Control 2 **$002D**

	Bit 7	6	5	4	3	2	1	Bit 0
	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
RESET:	0	0	0	0	0	0	0	0

TIE — Transmit Interrupt Enable
0 = TDRE interrupts disabled
1 = SCI interrupt requested when TDRE status flag is set

TCIE — Transmit Complete Interrupt Enable
0 = TC interrupts disabled
1 = SCI interrupt requested when TC status flag is set

RIE — Receiver Interrupt Enable
0 = RDRF and OR interrupts disabled
1 = SCI interrupt requested when RDRF flag or the OR status flag is set

ILIE — Idle Line Interrupt Enable
0 = IDLE interrupts disabled
1 = SCI interrupt requested when IDLE status flag is set

TE — Transmitter Enable
0 = Transmitter disabled
1 = Transmitter enabled

RE — Receiver Enable
0 = Receiver disabled
1 = Receiver enabled

RWU — Receiver Wakeup Control
0 = Normal SCI receiver
1 = Wakeup enabled and receiver interrupts inhibited

SBK — Send Break
0 = Break generator off
1 = Break codes generated as long as SBK = 1

SCSR — SCI Status Register **$002E**

	Bit 7	6	5	4	3	2	1	Bit 0
	TDRE	TC	RDRF	IDLE	OR	NF	FE	—
RESET:	1	1	0	0	0	0	0	0

TDRE — Transmit Data Register Empty Flag

This flag is set when SCDR is empty. Clear the TDRE flag by reading SCSR and then writing to SCDR.

0 = SCDR busy
1 = SCDR empty

TC — Transmit Complete Flag

This flag is set when the transmitter is idle (no data, preamble, or break transmission in progress). Clear the TC flag by reading SCSR and then writing to SCDR.

0 = Transmitter busy
1 = Transmitter idle

RDRF — Receive Data Register Full Flag

RDRF is set if a received character is ready to be read from SCDR. Clear the RDRF flag by reading SCSR and then reading SCDR.

0 = SCDR empty
1 = SCDR full

IDLE — Idle Line Detected Flag

This flag is set if the RxD line is idle. Once cleared, IDLE is not set again until the RxD line has been active and becomes idle again. The IDLE flag is inhibited when RWU = 1. Clear IDLE by reading SCSR and then reading SCDR.

0 = RxD line is active
1 = RxD line is idle

OR — Overrun Error Flag

OR is set if a new character is received before a previously received character is read from SCDR. Clear the OR flag by reading SCSR and then reading SCDR.

0 = No overrun
1 = Overrun detected

NF — Noise Error Flag

NF is set if majority sample logic detects anything other than a unanimous decision. Clear NF by reading SCSR and then reading SCDR.

0 = Unanimous decision
1 = Noise detected

FE — Framing Error

FE is set when a zero is detected where a stop bit was expected. Clear the FE flag by reading SCSR and then reading SCDR.

0 = Stop bit detected
1 = Zero detected

Bit 0 — Not implemented

Always reads zero

SCDR — SCI Data Register **$002F**

	Bit 7	6	5	4	3	2	1	Bit 0
	R7/T7	R6/T6	R5/T5	R4/T4	R3/T3	R2/T2	R1/T1	R0/T0
RESET:	U	U	U	U	U	U	U	U

NOTE

SCI receive and transmit data are double buffered. Reads of SCDR access the receive data buffer and writes access the transmit data buffer.

9 Serial Peripheral Interface

The SPI allows the MCU to communicate synchronously with peripheral devices and other microprocessors. When configured as a master, data transfer rates can be as high as one-half the E clock rate (1.5 Mbits per second for a 3 MHz bus frequency). When configured as a slave, data transfers can be as fast as the E clock rate (3 Mbits per second for a 3 MHz bus frequency).

When the SPI is enabled, all pins that are defined by the configuration as inputs are inputs regardless of the state of the DDR bits for those pins. All pins that are defined as outputs will be outputs only if the DDR bits for those pins are set to one. Any SPI output whose corresponding DDR bit is cleared to zero can be used as a general-purpose input. If the SPI system is in master mode and DDRD bit 5 is set to one, the port D bit 5 pin becomes a general-purpose output instead of the $\overline{SS}$ input to the SPI system. The MODF mode error flag function for which $\overline{SS}$ was used becomes disabled to avoid interference between the general-purpose output function and the SPI system.

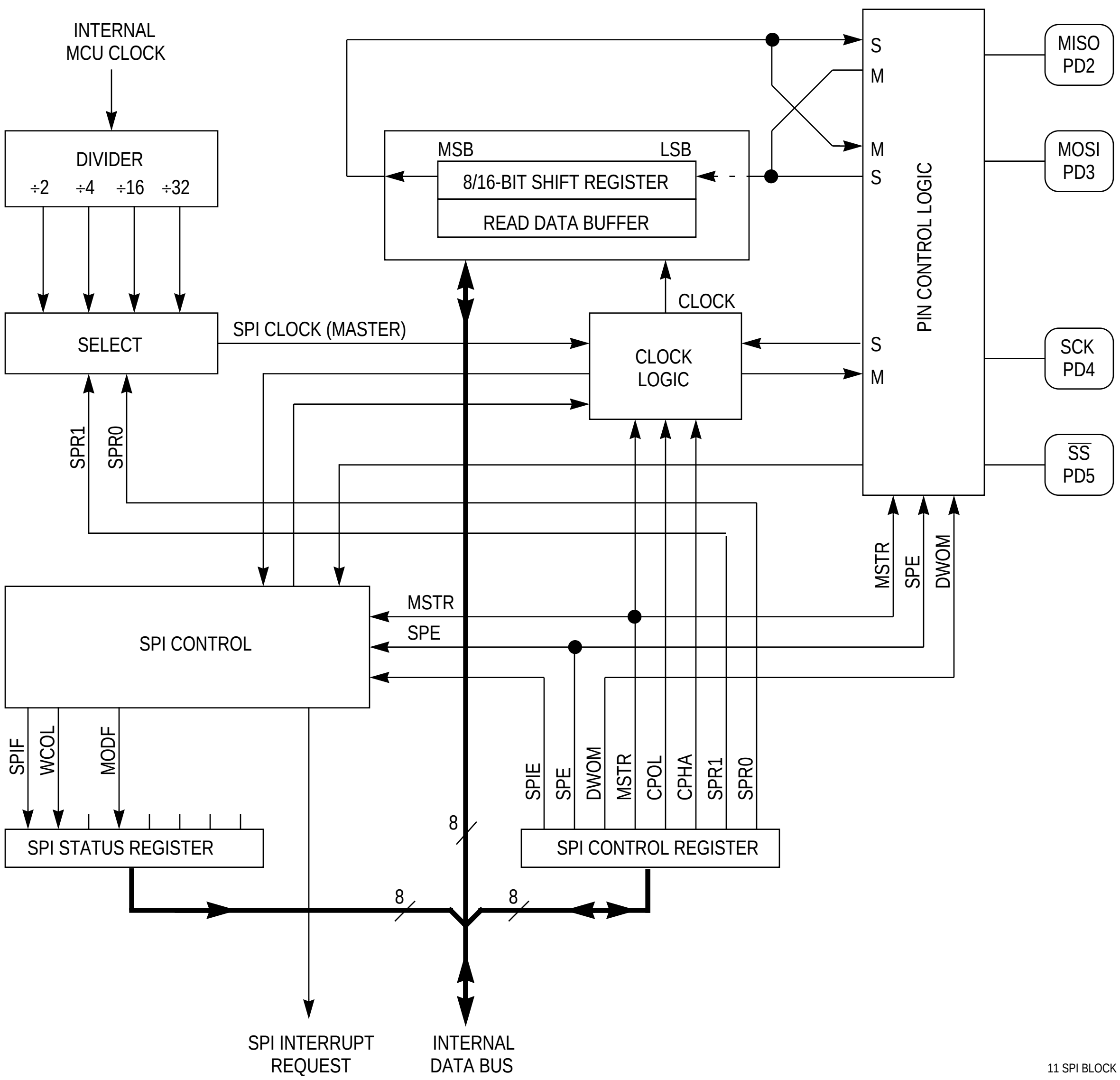

Figure 12 SPI Block Diagram

SPCR — Serial Peripheral Control Register **$0028**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIE	SPE	DWOM	MSTR	CPOL	CPHA	SPR1	SPR0
RESET:	0	0	0	0	0	1	U	U

SPIE — Serial Peripheral Interrupt Enable
0 = SPI interrupts disabled
1 = SPI interrupts enabled

SPE — Serial Peripheral System Enable
0 = SPI off
1 = SPI on

DWOM — Port D Wired-OR Mode Option for Port D Pins PD[5:2]
0 = Normal CMOS outputs
1 = Open-drain outputs

MSTR — Master Mode Select
0 = Slave mode
1 = Master mode

CPOL, CPHA — Clock Polarity, Clock Phase
Refer to Figure 13.

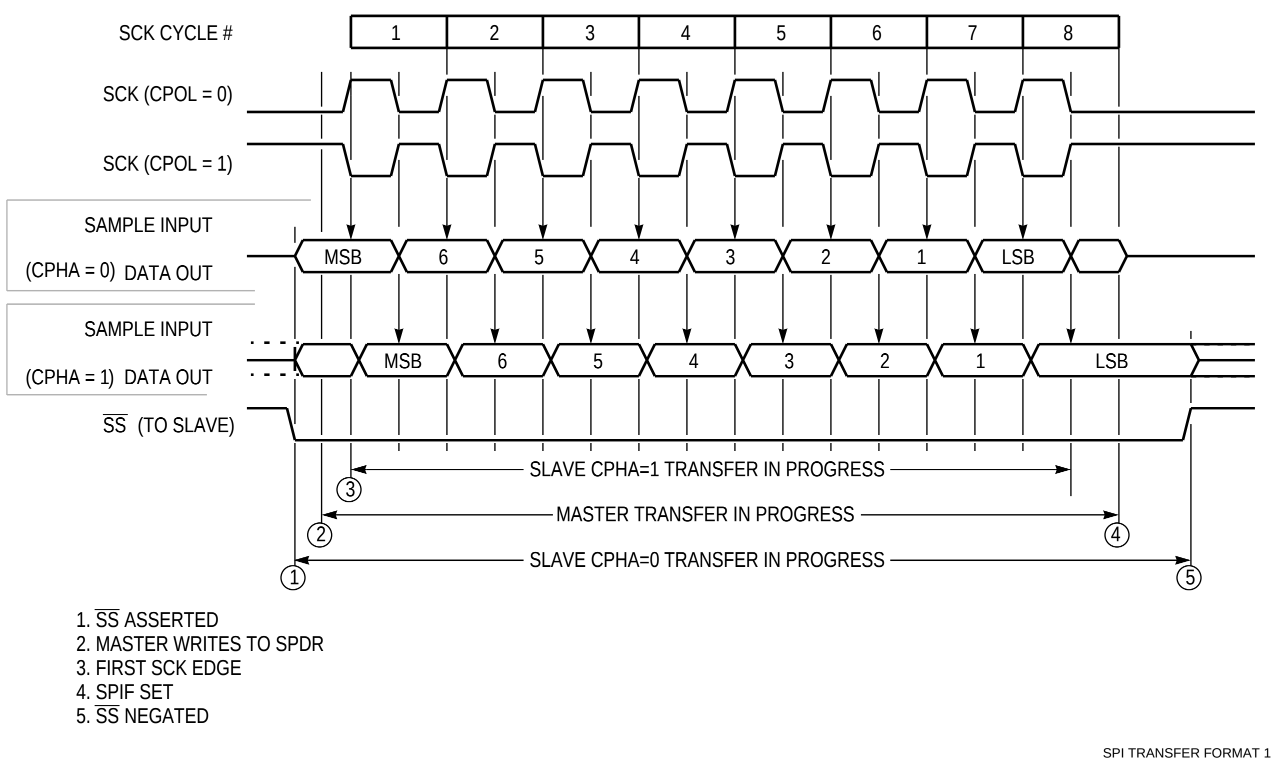

Figure 13 SPI Transfer Format

SPR[1:0] — SPI Clock Rate Selects

Table 9 SPI Clock Rate Selects

SPR[1:0]	Divide E Clock By	SPI Baud Rate at E = 1 MHz	SPI Baud Rate at E = 2 MHz	SPI Baud Rate at E = 3 MHz
0 0	2	500 kHz	1.0 MHz	1.5 MHz
0 1	4	250 kHz	500 kHz	750 kHz
1 0	16	125 kHz	125 kHz	375 kHz
1 1	32	62.5 kHz	62.5 kHz	187.5 kHz

SPSR — Serial Peripheral Status Register **$0029**

	Bit 7	6	5	4	3	2	1	Bit 0
	SPIF	WCOL	—	MODF	—	—	—	—
RESET:	0	0	0	0	0	0	0	0

SPIF — SPI Transfer Complete Flag

This flag is set when an SPI transfer is complete (after eight SCK cycles in a data transfer). Clear this flag by reading SPSR, then access SPDR.

0 = No SPI transfer complete or SPI transfer still in progress
1 = SPI transfer complete

WCOL — Write Collision Error Flag

This flag is set if the MCU tries to write data into SPDR while an SPI data transfer is in progress. Clear this flag by reading SPSR, then access SPDR.

0 = No write collision error
1 = SPDR written while SPI transfer in progress

Bit 5 — Not implemented

Always reads zero

MODF — Mode Fault (Mode fault terminates SPI operation)

Set when $\overline{SS}$ is pulled low while MSTR = 1. Cleared by SPSR read followed by SPCR write.

0 = No mode fault error
1 = $\overline{SS}$ pulled low in master mode

Bits [3:0] — Not implemented

Always read zero

SPDR — SPI Data **$002A**

Bit 7	6	5	4	3	2	1	Bit 0
Bit 7	6	5	4	3	2	1	Bit 0

SPI data is double buffered in, single buffered out.

NOTES

How to reach us:

USA/EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447
MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE (602) 244-6609
INTERNET: http://Design-NET.com
JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315
HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298